UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,064	10/30/2003	Peter Henry Mahowald	10030676-1	8140

57299 7590 06/15/2006

AVAGO TECHNOLOGIES, LTD.
P.O. BOX 1920
DENVER, CO 80201-1920

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,064	MAHOWALD, PETER HENRY	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *9-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/697064 Attorney's Docket #: 10030676-1
Filing Date: 10/30/2003

Applicant: Mahowald

Examiner: Alexander Williams

Applicant's election with traverse of Group I (device claims 1-8) filed 4/21/06 is acknowledged.

This application contains claims 9-14 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR ∋ 1.144 & MPEP ∋ 821.01).

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim language in claims 1-8 must be shown or the feature(s) canceled from the claim(s). For example, in claim 1, Applicant claims a first substrate; an optoelectronic device formed on the first substrate, the optoelectronic device having a frequency response; and a matching circuit formed on the first substrate and coupled to the optoelectronic device to change its frequency response. No figures no this complete claimed structure. Where is the apparatus comprising a first substrate with the optoelectronic device on the first substrate and a matching circuit on the first substrate and coupled to the optoelectronic device? The drawings fail to show a first or second substrate. Where are they shown in any of the drawings? No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The disclosure is objected to because of the following informalities:

Appropriate correction is required.

The drawings are objected to because fail to show the claimed figures of the claimed structure.

Correction is required.

Claims 1 to 8 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1-8, it is unclear and confusing to what is meant since the claimed structures are not shown in the drawing. Where are the first and second substrates in any of the drawings? What features in the drawings show the claimed structures?

Any of claims 1 to 8 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1, **insofar as it can be understood**, is rejected under 35 U.S.C. § 102(e) as being anticipated by Aikawa et al. (U.S. Patent Application Publication # 2003/0122628 A1).

1. Aikawa et al. (figures 1 to 18) specifically figure 12c show an apparatus comprising: a first substrate **3**; an optoelectronic device **2A** formed on the first substrate, the optoelectronic device having a frequency response; a matching circuit **7** formed on the first substrate and coupled to the optoelectronic device to change its frequency response.

[0064] In this event, since low impedance Gunn diode 2 is connected in a central region of coplanar line resonator circuit 7 in which the current substantially reaches the maximum in the resonance mode and the voltage reaches the minimum, impedance matching can be readily achieved between Gunn diode 2 and resonator circuit 7 without additionally providing an extra matching circuit or matching line. In addition, since signal line 7A and ground conductor 4 of coplanar line resonator circuit 7 are disposed on the same principal surface of substrate 3, Gunn diode 2 can be readily mounted on this principal surface. Moreover, elimination of the need for a via hole formed through substrate 3 contributes to a reduced circuit loss and an increased oscillation output.

Claims 1 to 8, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Reedy et al. (U.S. Patent # 6,583,445 B1).

1. Reedy et al. (figures 1 to 6) specifically figure 2B show an apparatus **10** comprising: a first substrate **11**; an optoelectronic device **20** formed on the first substrate, the optoelectronic device having a frequency response; a matching circuit formed on the first substrate and coupled to the optoelectronic device to change its frequency response.

2. An apparatus as in claim 1, Reedy et al. further comprising: a driver circuit **110,33** that communicates with and controls the optoelectronic.

3. An apparatus as in claim 2, Reedy et al. further comprising: a second substrate, wherein the driver circuit is formed on the second substrate.
4. An apparatus as in claim 3, Reedy et al. show wherein the matching circuit is selected to match the frequency response of the optoelectronic device to the driver circuit for optimal performance.
5. An apparatus as in claim 4, Reedy et al. show wherein the optoelectronic device is a Vertical Cavity Surface Emitting Laser (VCSEL).
6. An Apparatus as in claim 4, Reedy et al. show wherein the optoelectronic device is an edge-emittting diode.
7. An apparatus as in claim 4, Reedy et al. show wherein the matching circuit includes a passive device **33** from the group consisting of inductors, capacitors, resistors, stubs, and **diodes**.
8. An apparatus as in claim 4, Reedy et al. show wherein the optoelectronic device is flip-chip mounted to the auxiliary circuit.

(11) Operation block 2 illustrates the fabrication, on the high quality ultrathin silicon-on-sapphire composite substrate, of the electronic circuits required to control optoelectronic devices, e.g., drivers for a VCSEL, amplifiers for the input from a photodetector, etc., using fabrication techniques well-known to microelectronics practitioners. Such techniques are described in standard references such as Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET (S. Wolf, Lattice Press, Sunset Beach, Calif.: 1995); VLSI Technology, Second Edition (Edited by S. M. Sze, McGraw-Hill, New York, 1988). Design of such silicon-based electronic circuitry is readily accomplished by integrated circuit design practitioners. Fabrication technology for such silicon-based electronic circuitry is also well-known.

(12) In some configurations of the invention, the silicon electronic circuitry includes VCSEL drivers (e.g., CMOS) for powering and controlling surface-emitting lasers. The VCSEL drivers are integrated with the VCSEL lasers by flip-chip bonding. A CMOS VCSEL driver has been described and analyzed by Lawler et al. (Lawler et al., "CMOS Drive Circuit for Hybrid Optical Interconnects," Proc. 2.sup.nd Intl. Workshop on Design of Mixed-Mode Integrated Circuits and Applications," Guanajuato, Mexico, p. 29-32, Jul.

27-29, 1998; Lawler, B. "CMOS Drive Circuit for Opto-Electronic Readout of Image Sensors," Proc. 1999 IEEE Intl. Symp. Circuits and Systems, vol. V,pp. V124-V127, Orlando, Fla., May 30, 1999).

(38) In these examples, the electronic circuits in silicon may include CMOS devices. Typical CMOS devices include VCSEL drivers, receiver circuits for photodetectors, and other signal/data processing and switching circuits. Typical optoelectronic devices may include light-emitting devices such as lasers and diodes, light detecting devices such as photodetectors, and light modulators, such as quantum well modulators. Often, the light emitting optoelectronic devices are fabricated in III-V materials; and the light detecting devices are fabricated in III-V, IV and II-VI materials. For infrared and visible light, the light emitting devices are commonly on GaAs substrates and light detecting devices are fabricated in GaAs, InGaAs, Si, Ge. In the practice of the present invention, it is an advantage that optoelectronic devices of more than one type of material may be incorporated into the hybrid module. For example, an advantageous combination comprises a II-VI based photodetector input, fabricated for example in HgCdTe, as input, in combination with a III-V based VCSEL output, fabricated for example in GaAs.

(52) To summarize, advantages that are specific to hybrid structures such as those depicted schematically in FIGS. 2A, 2B, 2C, 3B, 3C, 3D, 3E and 4 include: Optical transparency of the sapphire substrate allows easy optical access to optoelectronic devices, for example, transmitters such as VCSELs may be top-emitting and/or bottom-emitting and receivers such as photodetectors may be frontside illuminated and/or backside illuminated; Thermal properties of sapphire dissipate heat from the electronic and optoelectronic devices more efficiently. Good thermal diffusivity avoids hot spots; Sapphire is very well matched to GaAs in thermal coefficient of expansion. This thermal match makes the hybrid device combination much more robust; Good dielectric properties of sapphire reduce or eliminate substrate coupling and substrate loading effects in the electronic circuits; Physically small size, because flip-chip bonding reduces number of individual separate device structures, which previously would have been connected by bonding wires; Reliability is improved, since solder bonds are much less prone to failure than bond wires, whose connection to substrate is one of the most physically fragile

points of an IC module; The combination of flip-chip bonding (i.e., elimination of bonding wires and conductive vias) and fabrication in ultra-thin silicon-on-sapphire composite substrates significantly reduces electrical parasitic effects; and Cost and yield are improved, because the CMOS circuitry and the optoelectronic devices can be fabricated in arrays for bonding.

Claims 1 to 4 and 6 to 8, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Eden et al. (U.S. Patent Application Publication # 2002/0195662 A1).

1. Eden et al. (figures 1 to 19) specifically figure 5 show an apparatus comprising: a first substrate **78**; an optoelectronic device **72** formed on the first substrate, the optoelectronic device having a frequency response; a matching circuit formed on the first substrate and coupled to the optoelectronic device to change its frequency response.

2. An apparatus as in claim 1, Eden et al. further comprising: a driver circuit **180** that communicates with and controls the optoelectronic.

3. An apparatus as in claim 2, Eden et al. further comprising: a second substrate **76**, wherein the driver circuit is formed on the second substrate.

4. An apparatus as in claim 3, Eden et al. show wherein the matching circuit is selected to match the frequency response of the optoelectronic device to the driver circuit for optimal performance.

6. An Apparatus as in claim 4, Eden et al. show wherein the optoelectronic device is an edge-emittting diode.

7. An apparatus as in claim 4, Eden et al. show wherein the matching circuit includes a passive device from the group consisting of inductors, capacitors, resistors, stubs, and diodes.

8. An apparatus as in claim 4, Eden et al. show wherein the optoelectronic device is flip-chip mounted to the auxiliary circuit.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/349,82,80,81,138,e31.054,e23.079,e25.015,e23.062, e29.116,e29.136	6/7/06
Other Documentation: foreign patents and literature in 257/349, 82,80,81,138, e31.054,e23.079,e25.015,e23.062,e29.116,e29.136	6/7/06
Electronic data base(s): U.S. Patents EAST	6/7/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/7/06